REMARKS

A. GENERALLY

Claims 1-6 and 8-14 remain in the Application. Claims 1-6 and 8-10 have been amended. Claim 7 has been canceled. Claims 13 and 14 have been added. No new matter has been added.

B. CLAIM REJECTIONS

1. Claim Rejections Under 35 U.S.C. §112¶2

Claims 1, 4, 7, 8 and 9 have been rejected under 35 U.S.C. §112¶2 as being indefinite. The rejections stem from the use of "and/or" in the claims. Applicant has amended the claims to remove "and/or" from the claims. Based on the foregoing, Applicant submits that claims 1, 4, 7, 8 and 9 as currently listed are in proper form and requests that the rejections of these claims be withdrawn.

2. Claim Rejections Pursuant to 35 U.S.C. § 102

Claims 1-10 and 12 have been rejected under 35 U.S.C. 102(a) as being anticipated by U.S Patent 5,504,701 issued to Takahashi (hereinafter, "Takahashi").

Claim 1 (as amended) recites the following limitations:

> 1. (Currently Amended) A method for securing data of a data carrier comprising:
>
> determining a current state of a memory, wherein the memory comprises a plurality of memory cells and wherein the current state of the memory is selected from the group consisting of an active state and a quiet state and wherein in the active state the data of the data carrier is accessible and wherein in the quiet state the data of the data carrier is inaccessible;
>
> if the memory is in the active state, then determining a current state of a memory cell, wherein the current state of the memory cell is selected from the group consisting of a programmed state and an unprogrammed state; and
>
> if the current state of the memory cell is the unprogrammed state, then selecting the memory cell and programming the selected memory cell to change the current state of the memory cell to the programmed state, wherein the memory cell assumes an irreversible memory state as a result of the programming and wherein the memory enters the quiet state.

The limitations of claim 1 (as amended) are directed to securing data in a data carrier based on the state of a memory. The state of a memory is changed by programming the memory cell from an unprogrammed state to a programmed stated. The programmed state of a cell is irreversible.

Takahashi describes a card in which the number of erase (initialization) cycles are limited and in which the number of remaining erasures are stored in an EPROM or recorded in a fuse ROM:

> An EPROM (Electrically Programmable ROM) 200 for counting the number of initialization of the user memory 100, is connected to the erase control logic 210. In the first embodiment, not the number of times of erase itself, but the remaining number of times allowing an erase operation, is stored in the EPROM 200 and, when the data (the remaining number) stored in the EPROM 200 becomes 0, the erase control logic 210 inhibits the erase operation. For this reason, the EPROM 200 has memory cells the number of which corresponds to the number of times the prepaid card can be initialized, and inverts data of the memory cells whenever the card is initialized. This initialization can be continued until data of all the memory cells are inverted. It should be noted that the EPROM 200 differs from the user memory 100 in that it is incapable of being rewritten (or initialized). The EPROM 200 can be replaced with a fuse ROM having fuses the number of which corresponds to the number of times allowing the initialization, to cut off the fuses every initialization. In either case, it is necessary that the EPROM 200 cannot be accessed (or rewritten) by the external terminal device. The card can thus be prevented from being initialized (reused) over a predetermined number of times and can be prevented from being used dishonestly without restriction. (Takahashi, Col. 3, line 52 through Col. 4, line 8.)

The system described by Takahashi operates by inhibiting an erase control signal:

> The output of the OR gate 213 is supplied to a first input terminal of an AND gate 214. The output signal C.sub.0 of the timing control circuit 212 is inverted, and the inverted signal is supplied to a second input terminal of the AND gate 214. The output signal of the AND gate 214 is input to the address decoder 120 as an erase control signal ERS. When the signal ERS is equal to "0", data of the user memory 100 is inhibited from being erased (initialized). When ERS is equal to "1", the data is allowed to be erased (initialized). (Takahashi, Col. 4, lines 41-49.)

Takahashi thus describes a memory that may be accessed and rewritten (erased) a predetermined number of times. Takahashi does not teach or reasonably suggest a memory that can alternate between at least two states. That is, the memory of Takahashi is described as being in a writable state until the predetermined number of erasures is exceeded. In contrast, the limitations of claims 1 and 5 (as amended) are drawn to a method and an integrated circuit that can toggle between an active state (allowing access to data stored in a data carrier) and a quiet state (denying access to the data stored in the data carrier).

Claims 1 and 5 (as amended) thus recite limitations not taught or reasonably suggested by Takahashi and are therefore, not anticipated by Takahashi.

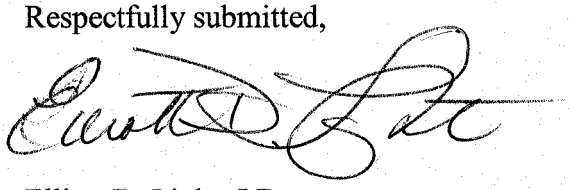
Claim 2-4 (as amended) depend from claim 1 and recite all of the limitations of that base claim. Based on the foregoing, claims 2-4 recite limitations not taught or reasonably suggested by Takahashi and are not anticipated by that reference.

Claims 6 and 8-14 depend from claim 5 and recite all of the limitations of that base claim. Based on the foregoing, claims 6 and 8-14 recite limitations not taught or reasonably suggested by Takahashi and are not anticipated by that reference.

C. CONCLUSION

Applicant respectfully submits that the claims as currently listed are in condition for allowance. Applicant requests that this response be entered and that the current rejections of the claims now pending in this application be withdrawn in view of the above amendments, remarks and arguments.

Respectfully submitted,



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